

BACHELOR THESIS

- WORKGROUP TERAHERTZ / PHOTONIK, PROF. DR. V. KROZER -

Title: Implementation and optimization of a clock distribution in a digital integrated circuit

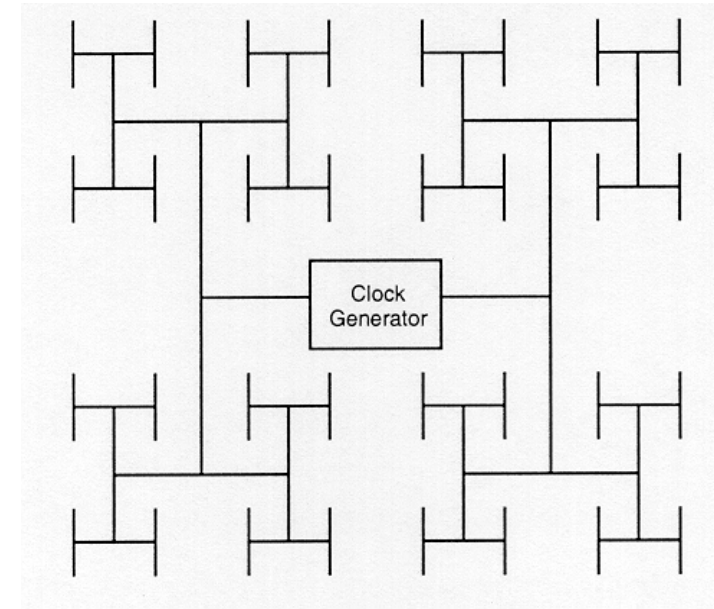
A very important issue in the design of a synchronous digital circuit is the distribution of the clock signal that ensures that all gates on the chip work correctly. For circuits operating at high frequencies this aspect becomes more critical and therefore the clock skew has to be controlled very carefully. In this thesis a clock tree (for instance a H-Tree) shall be implemented/optimized for a *Direct Digital Synthesizer (DDS)*.

Tasks:

- Comparison of different options of implementing a clock tree
- Implementation and optimization of a clock tree for a DDS

Qualifications:

- familiar with basic electrical engineering
- experienced in working with simulation tools (like ADS, Cadence Virtuoso, SPICE..) would be advantageous



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Start: From now on